THE INVENTION CLAIMED IS:

1. A method for maintaining control structure coherency comprising:

writing a pointer to a control structure in a hardware update list while one or more portions of the control structure are accessed by hardware during a hardware update operation; and

delaying a software access to one or more portions of the control structure during a software update operation while the pointer to the control structure is on the hardware update list.

2. The method of claim 1 further comprising removing the pointer to the control structure from the hardware update list after the one or more of the portions of the control structure accessed by the hardware during the hardware update operation are no longer accessed by the hardware.

3. The method of claim 1 wherein writing the pointer to the control structure in the hardware update list while one or more portions of the control structure are accessed by hardware includes writing the pointer to the control structure in the hardware update list while all portions of the control structure are accessed by the hardware during the hardware update operation.

4. The method of claim 1 wherein the software update operation includes updating a field of the control structure.

5. The method of claim 1 wherein the pointer represents at least a portion of an address of the control structure.

6. The method of claim 1 wherein the hardware update list is stored in hardware.

7. The method of claim 6 wherein the hardware update list is stored in at least one of memory and registers.

8. The method of claim 1 wherein the hardware update list includes a plurality of entries.

9. The method of claim 1 wherein the control structure includes a control block.

10. The method of claim 9 wherein a control block includes a plurality of bytes of data.

11. The method of claim 9 wherein the control block includes information based on a cell or frame received by a network processor.

12. The method of claim 9 wherein the one or more portions of the control structure include one or more bytes of the control block.

13. The method of claim 1 wherein writing the pointer to the control structure in the hardware update list while one or more portions of the control structure are accessed by the hardware during the hardware update

operation includes writing the pointer to the control structure in the hardware update list while one or more pointers of the control structure are read from a memory, modified, and written back to the memory by the hardware during the hardware operation.

14. The method of claim 1 wherein delaying the software access includes monitoring a bus for at least one of a control signal and an address.

15. The method of claim 14 wherein delaying the software access includes rejecting software access to the bus while the pointer to the control structure is on the hardware update list.

16. The method of claim 14 wherein delaying the software access includes:

granting a request for the software access; and

delaying the software access while the pointer to the control structure is on the hardware update list.

17. The method of claim 1 wherein delaying the software access to one or more portions of the control structure while the pointer to the control structure is on the hardware update list includes delaying a software access caused by instructions executed on a processor of a network processor.

18. The method of claim 1 wherein delaying the software access to one or more portions of the control structure while the pointer to the control structure is on the hardware update list includes delaying at least one of

a read, a modify and a write operation performed by software on the one or more portions of the control structure while the pointer to the control structure is on the hardware update list.

19. An apparatus comprising:

hardware update logic adapted to couple to a memory controller of a network processor and adapted to interact with an at least one memory so as to:

write a pointer to a control structure stored in the at least one memory in a hardware update list while one or more portions of the control structure are accessed by the hardware update logic during a hardware update operation; and

delay a software access to one or more portions of the control structure during a software update operation while the pointer to the control structure is on the hardware update list.

20. The apparatus of claim 19 wherein the hardware update logic is further adapted to remove the pointer to the control structure from the hardware update list after the one or more of the portions of the control structure accessed by the hardware update logic during the hardware update operation are no longer accessed by the hardware.

21. The apparatus of claim 19 wherein the hardware update logic is adapted to detect the software access by employing the memory controller to monitor at least one of a control signal and an address on a bus.

22. The apparatus of claim 20 wherein the hardware update logic is adapted to delay the software access by employing the memory controller to reject software access to the bus while the pointer to the control structure is on the hardware update list.

23. The apparatus of claim 20 wherein the hardware update logic is adapted to delay the software access by employing the memory controller to:

grant a request for the software access; and

delay the software access while the pointer to the control structure is on the hardware update list.

24. A network processor system comprising:

at least one memory adapted to store a plurality of control structures;

a network processor comprising:

a memory controller coupled to the at least one memory;

hardware update logic coupled to the memory controller and adapted to interact with the at least one memory so as to:

write a pointer to a control structure in a hardware update list while one or more portions of the control structure are accessed by the hardware update logic during a hardware update operation; and

delay a software access to one or more portions of the control structure during a

software update operation while the pointer to the control structure is on the hardware update list.

25. The network processor system of claim 24 wherein the hardware update logic is further adapted to remove the pointer to the control structure from the hardware update list after the one or more of the portions of the control structure accessed by the hardware update logic during the hardware update operation are no longer accessed by the hardware.

26. The network processor system of claim 24 wherein the hardware update logic is adapted to detect the software access by employing the memory controller to monitor at least one of a control signal and an address on a bus.

27. The network processor system of claim 24 wherein the memory controller includes the hardware update logic.

28. The network processor system of claim 27 wherein the hardware update logic includes on-chip memory.

29. The network processor system of claim 24 further comprising a plurality of processors coupled to the memory controller using an internal bus.

30. The network processor system of claim 24 wherein the at least one memory includes a DRAM.